MCA DEGREE I SEMESTER EXAMINATION DECEMBER 2013

CAS 2102 COMPUTER ORGANISATION
(Regular and Supplementary – 2012 Revision)

Time: 3 Hours

Maximum Marks: 50

PART A
(Answer *ALL* questions)

$(15 \times 2 = 30)$

I.
  (a) Define MAR & MDR.
  (b) Convert the following into binary
    (i) $(12.34)_{10}$ (ii) $(45.25)_8$
  (c) What is the use of linkage register?

II.
  (a) What is interrupt latency?
  (b) What is centralized arbitration in DMA.
  (c) What is the significance of replacement algorithms in cache memory?

III.
  (a) Multiply 12 x –6 using Booth method.
  (b) Compare different bas organisations.
  (c) What is vertical and horizontal organisation of microinstructions.

IV.
  (a) Explain data hazards.
  (b) Compare micro controllers and microprocessors.
  (c) What is pipelining.

V.
  (a) Explain the working of a track ball.
  (b) Compare simplex and duplex communications.
  (c) Explain the classification of parallel structures.

PART B

$(5 \times 4 = 20)$

VI.   Write short note on subroutines.
OR
VII.   What are the different addressing modes?

VIII.   Explain different mapping functions in cache memory.
OR
IX.   Write short note on USB.

X.   What is an instruction? Write down the control sequence for the execution of the instruction. Add (R_1), R_2.
OR
XI.   Explain hardwired control with neat block diagram.

XII.   Write note on super scalar operations.
OR
XIII.   Explain the working of an embedded system with example.

XIV.   Compare synchronous and asynchronous transmission.
OR
XV.   Write note on Array Processors.

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