MCA.I/12.15.1095 Reg. No. | | | | | | | | |

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MCA DEGREE I SEMESTER EXAMINATION DECEMBER 2015

CAS 2102/2104 COMPUTER ORGANISATION

(Old Scheme – Supplementary)

Time: 3 Hours Maximum Marks: 50

PART A

(Answer ***ALL*** questions)

(15 × 2 = 30)

I. (a) Give difference methods to represent signed numbers.
(b) What do you mean by addressing mode? How is it important to determine the execution time of instructions?
(c) Give the operational concepts of JK, D and T flip flops.

II. (a) What is an interrupt? Give typical interrupts processing mechanism.
(b) How memory mapped I/O differ from I/O mapped I/O?
(c) Give the operation semiconductor RAM memory using BJT.

III. (a) Explain how subtraction of signed numbers can be implemented using adders.
(b) Explain different steps involved in execution of a complete instruction.
(c) Give brief notes on multiple-bus organisation.

IV. (a) Explain different data hazards.
(b) What is an embedded system? What are the characteristics of an embedded system?
(c) How are microcontroller differed from microprocessors?

V. (a) Write notes on RS-232C serial interface standard.
(b) Write notes on shared memory multiprocessor organisation.
(c) Explain how parallelism can be achieved in an uniprocessor system.

PART B

(5 × 4 = 20)

VI. Draw the basic structure of a Von Neumann architecture based micro computer system. Explain each components of this architecture.

OR

VII. Explain different types of addressing modes supported by typical microprocessors.

VIII. Explain the following bus architectures.
(i) PCI (ii) USB

OR

IX. Explain memory hierarchy with respect to a typical micro computer system.

X. Explain Boot's algorithm for multiplication with examples.

OR

XI. Explain hardwired and microprogrammed control units.

XII. What is super scalar architecture? Explain how this architecture improves the performance of a processing unit.

OR

XIII. Explain general architecture of a typical microcontroller.

XIV. Explain Flynn's classification of parallel computer architecture.

OR

XV. Explain memory organisation in multiprocessor systems.

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